

Software Defined Radio Development Platform V1.1, January 15th, 2006

Overview

SDR v1.1 is FPGA-based SDR development platform, based on Xilinx Virtex-2 technology, high speed analog to digital and digital to analog converters. It lends itself to various applications involving high speed data conversion requirements and massive DSP processing engine requirements. The board is supported by high speed PCI and USB2.0 interfaces, providing connectivity to a PC host. C/C++ and MATLAB APIs reduce the development time by enabling data transport and control logic functionalities to be implemented on the SDR platform, which are used in data sourcing and logging applications, large file or single register transfers, burst or continuous communications. SDR platform with supported firmware and software enables user to focus attention to the problem at hand, and not on development environment.

The Xilinx Virtex-II FPGA (Field Programmable Gate Array) is a high capacity, user reprogrammable logic device ideally suited for the implementation of many complex high speed DSP algorithms. The PCI-Local bus supports multiple modes of data transfer, whether initiated by the PC Host, or the user design. A/D and D/A conversions are provided by high speed 14-bit devices. Sampling rates are controlled by a flexible clock distribution circuitry, fully controllable by the user application.

Processing Engine

- FF1152 Xilinx Virtex-II FPGA, three- to eight-million gate (XC2V3000 to XC2V8000)
- Spartan XCS2



Analog Section

- 2 x 14-bit @ 105 MSPS sampling rate A/D
- 2 x 14-bit @ 150 MSPS sampling rate D/A

Data Interfaces

- PCI V2.2 via Spartan 2 Firmware
- USB 2.0 via Spartan 2 Firmware

On Board Memory

- 64 Megabyte DDR

Digital Ports

- 80 pin connector, compatible with Texas Instruments daughter board interfacing specification
- 32-pin array for debugging and additional digital interfacing

Clocks

- 1x fixed low-jitter clock source for FPGA

- 1x user-programmable (25MHz – 100MHz) clock source
- 1x clock source for PCI and interfacing
- 1x buffered external clock source
- Sampling clock for A/D and D/A: differential LVPECL, DCM selectable multiplication ratio

Connector for external power supply for stand alone mode

Configuration

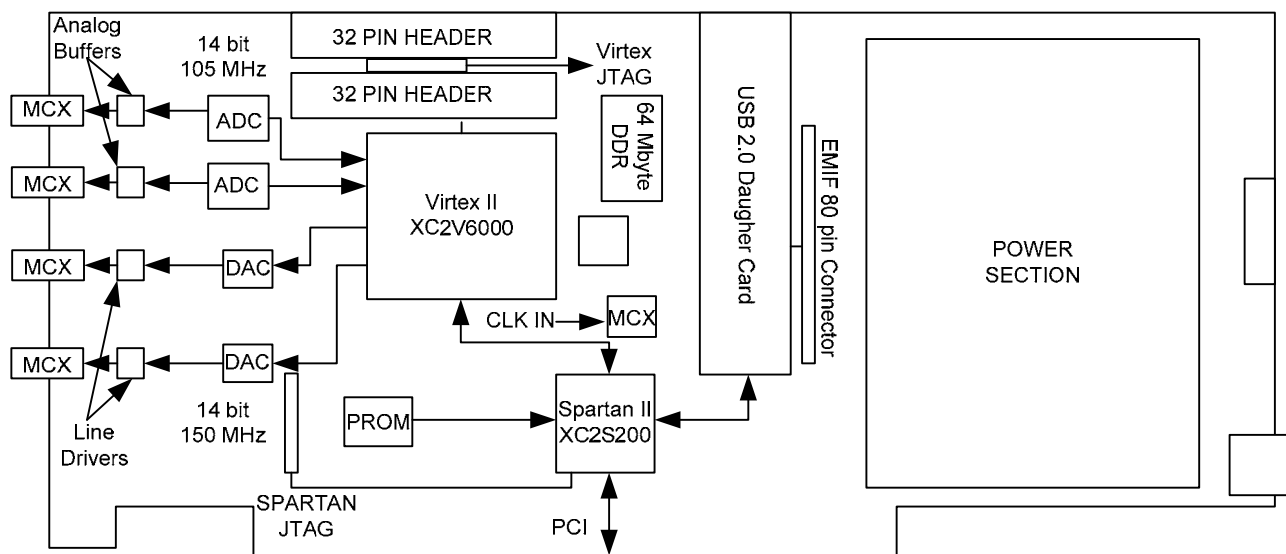
Virtex 2 FPGA configuration:

- from user application via PCI
- from user application via USB 2.0
- directly via JTAG

Power

Powered from PCI, HDD connector for additional power supply

Functional Diagram



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