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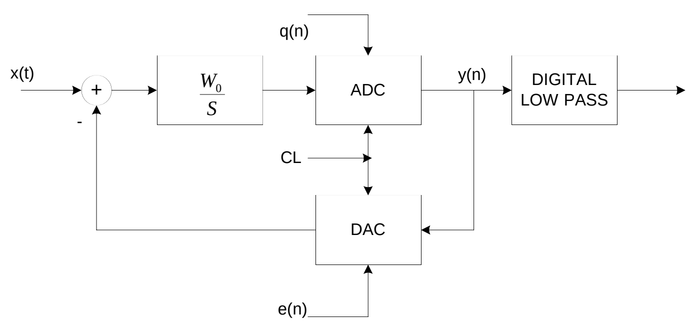
IMPROVED PERFORMANCE OF MULTI-BIT DELTA-SIGMA ANALOG TO DIGITAL CONVERTERS VIA REQUANTIZATION

ABSTRACT

System performance of an oversampled analog to digital converter (ADC) with feedback noise shaping is limited by the precision of the digital to analog converter ~AC) in the feedback path as well as by the fluter of integrators in the loop(s). Standard designs avoid the DAC precision problem by restricting the ADC and DAC to a single bit while stability and matching considerations limit systems to three loops. This limit in turn defines the oversample ratio for a given effective bandwidth and noise performance. We present a simple modification to the oversampled ADO which avoids these limitations via requantization in the feedback path of the original delta sigma loop structure. This modification results in greater dynamic range than is available from standard configurations.

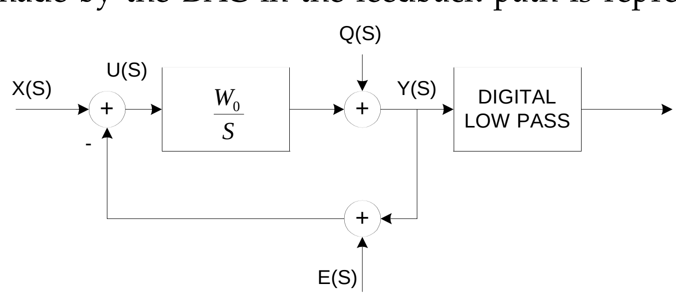
INTRODUCTION

The required components of a single loop delta-sig-ma converter are presented in Fig. 1. The ADC in the forward path and the DAC in feedback path operate at a sample rate far in excess of the input signal bandwidth. As we will see shortly, the spectrum of the ADO quantization error is shaped by the loop gain to suppress the spectral noise levels within the signal bandwidth at the expense of noise levels outside of the signal bandwidth. These out of band noise components are rejected by a high quality digital filter and the sariple rate is then reduced to the Nyquist rate for the filtered signal.



■ Figure 1. *Single loop delta-sigma converter*

The essential behavior of the converter can be determined by examining the multi-input, single output model of the feedback loop indicated in Fig. 2. Here the quantizing error made by the ADO in the forward path is represented by the additive term Q(s) while the reconstruction error made by the DAC in the feedback path is repre-



■ Figure 2. *Model of delta-sigma feedback loop*

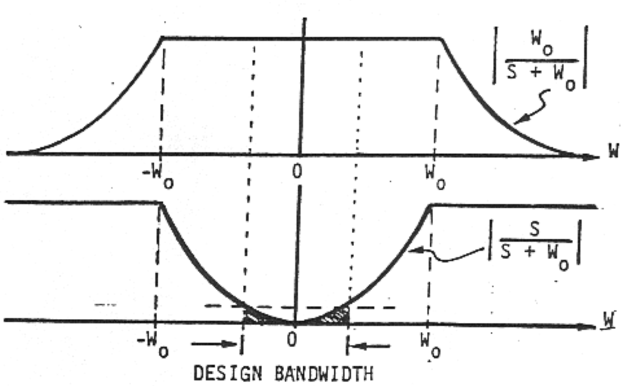
sented by the additive term E(s).
As indicated respectively in (1a) and (1b) the integrator operates on the difference between the input X(s) and the reconstructed output Y(s)+E(s) while the integrator output is presented to the ADC to form the loop output Y(s). Combining (1a) and (1b) and solving for Y(s) yields the standard delta-sigma loop equations:

$$U(s) = X(s) - [Y(s) + E(s)] \quad (1a)$$

$$Y(s) = \left[\frac{W_0}{s}\right] U(s) + Q(s) \quad (1b)$$

$$Y(s) = \frac{W_0}{s + w_0}[X(s) - E(s)] + \frac{s}{S + W_0} Q(s) \quad (1c)$$

We first recognize that the loop is stable (an important check before we continue) We then note that the noise component of the ADC, Q(s), is filtered by the zero at zero frequency but that the noise component of the DAC is not similarly reduced but rather experiences the same gain as the input signal. This latter observation means that if the system is to exhibit a specified level of noise performance, equivalent to say 16-bits, the DAC must exhibit this same level of performance. This is an exceedingly difficult task for a multi-level DAC which is why delta-sigma loops are implemented with one-bit converters.
The frequency responses of the two terms in (1c) are shown in Fig. 3. here the design bandwidth of the loop (hence the lowpass filter following the loop) is indicated as that band for which the noise level is less than the specified noise threshold.
We now present a simple modification of the standard delta-sigma loop which changes the behavior of E(s) the error component of the DAC feedback signal.



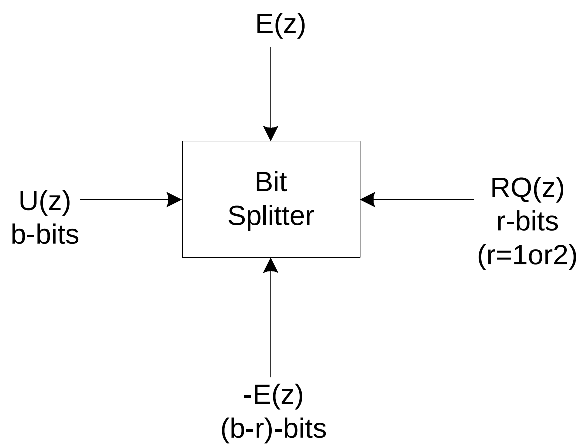
■ Figure 3. *Spectral gains for signal and for quantizer components*

MODIFIED FEEDBACK PATH

We can reduce the variance of the quantizing error, Q(s), by Using a multi-bit quantizer in the feedforward path of the delta-sigma loop. To take advantage of these additional bits in the feedforward path the traditional loop architecture requires that the number of bits in the feedback DAC must also be increased. The difficulty in fabricating a multi-bit DAC with the precision of the composite loop, to control the feedback error E(s), is so great that this is not an acceptable option.
We are thus faced with conflicting preferences; we desire a multibit ADC in the feedforward path but require a one (or two) bit DAC in the feedback path. A two bit DAC exhibits a reduced noise power density by including a zero level as well as the standard positive and negative levels. 1mw can we simply convert the multi-bit ADC output to a one or two-bit DAC feedback signal? One option that doesn't work is to simply discard the lower order bits of the ADC and merely use the most significant bit(s) as the feedback signal. This process requantizes the feedback signal (before converting back to analog) by truncating the lower order bits and thus does not use the precision of additional bits in the loop.
We choose a more desirable requantization scheme. We first realize that the feedback signal does not have to exhibit the system precision over the full bandwidth of the loop but rather over the restricted bandwidth we have called the design bandwidth, We can use an auxiliary feedback loop in the feedback path to reshape the spectrum of the feedback error signal during the requantization. The truncation error made by discarding the lower order bits is a known quantity and can

thus be used in its own error feedback loop.

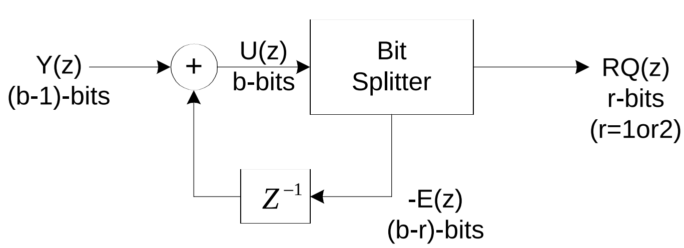
The bit splitter is a meworyless processing block Fig. 4, which takes a b-bit input word, u(n), and produces both an r-bit, (where r = 1 or 2), output word rq(n) corresponding to the DAC output levels and a (b-r)-bit error word which we will later process. This error word, -e(n) is the difference between the input u(n) to the bit splitter and the output rq(m). Both rq(n) and -e(n) are obtained for two's complement in the r=1 case by a simple split of u(n) and one bit inversion.



■ Figure 4. *Bit splitter block*

The bit splitter error is returned to the input to be spectrally shaped in a discrete feedback loop very much like that of the delta-sigma loop as shown in Fig. 5. we refer to this completed loop as a requantizer.

In the noise shaping loop the primary output of the requantizer RQ(z) is the quantized version of the sum of its input Y(z) and the error output formed during the precious cycle $z^{-1}E(z)$. These relationships are seen in (2a) and (2b) where they are combined to form the noise shaped output (2c).



■ Figure 5. *Noise shaping requantizer loop*

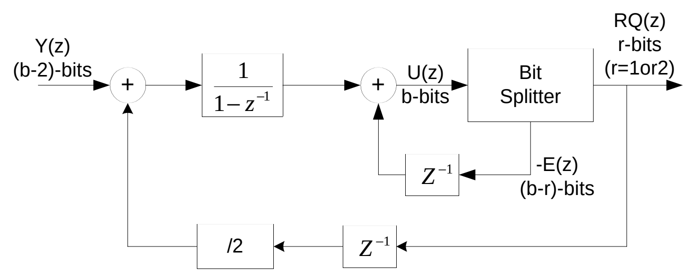
$$U(s) = Y(z) - z^{-1}E(z) \qquad \text{(2a)}$$

$$RQ(z) = U(z) + E(z) \qquad \text{(2b)}$$

$$RQ(z) = Y(z) + E(z)[1 - z^{-1}] \qquad \text{(2c)}$$

We see that the one (or two) bit requantized data RQ(z) in Fig. 5 is spectrally shaped by the zero at DC of the discrete loop much as the shaping that occurs in the analog delta-sigma loop. As with the delta-sigma loop, we can obtain enhanced performance of the discrete equivalent with multiple or cascade loops as indicated for instance in (2) and shown in Fig. 6.

$$RQ(z) = Y(z) + E(z)[1 - z^{-1}]^2 \qquad \text{(3)}$$



■ Figure 6. *Cascade requantizer loop*

In order to bound the magnitude of U(z) , the input to the bit splitter, RQ(z) is fed back to the summing junction with a hard-wired right shift (divide by 2). This enables input Y(z) to the second order requantizer to be of (b-2)-bit word length. This necessary division by two only slightly degrades the spectral noise shape. Also note that the post shifted RQ(z) is still of a higher bit position than the MSB of the input, Y(z) such that the difference can be made without logic.

This discrete requantizer loop is placed in the feedback path of the delta-sigma loop to permit a (b-2) -bit ADC to operate in the feedforward path with a one (or two) bit DAC operating in the feedback path. This is shown in Fig. 8.

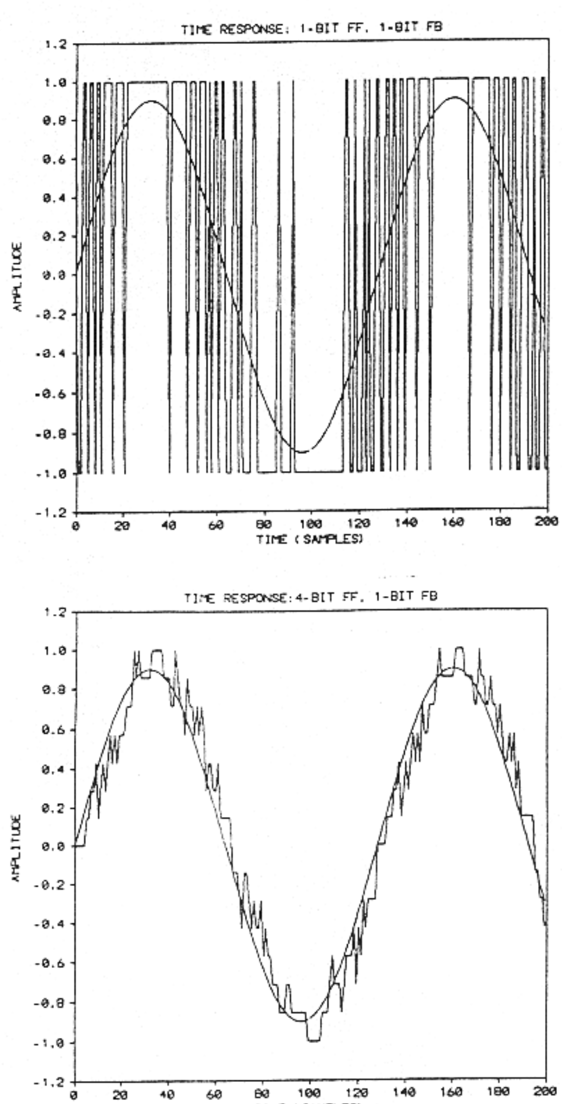
Because we have a multi-bit ADO in the feedforward path we have the option to clock the ADC at a lower sampling rate than the requantizer while remaining within the overall loop SNR limits imposed by the RQ and DAC.

CONCLUSIONS

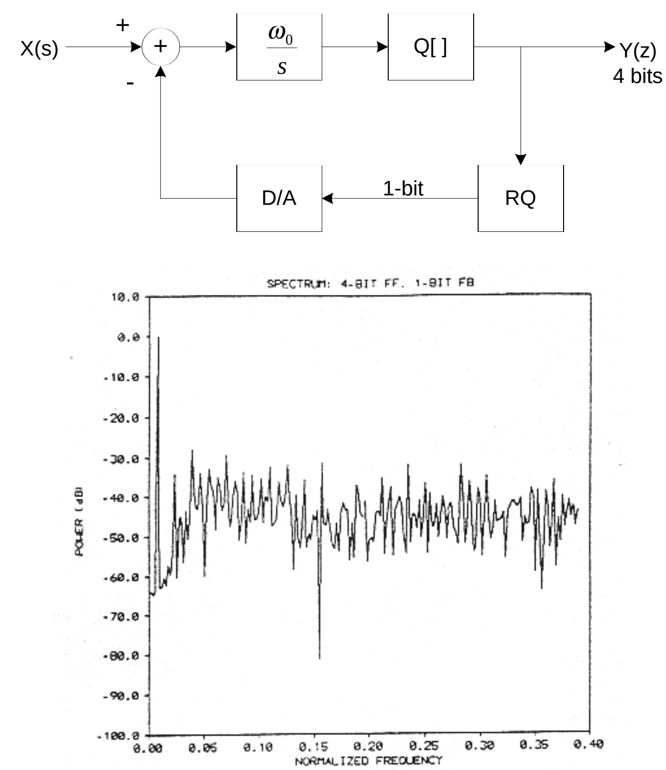
We have described a technique to improve the dynamic range of delta- sigma converters. The use of a noise shaping loop in the feedback path of the converter permits a multi-bit quantizer in the forward path and a one or two bit quantizer in the return path. Two benefits accrue to the use of the multibit ADC in the loop, both of which are due to the reduced variance of the qnantizer noise. The first benefit is an increase in design bandwidth for a given sample rate and order of loop. The second is a relaxed specification for the out of band attenuation of digital lowpass filter following the converter.

An example of the performance improvement to be had by this modification to the loop is to be seen in Fig. 7. here are shown the loop time response for a one and four bit ADO in the forward path both operating with a requantizer loop in the return path feeding a one bit DAC.

A prototype was constructed utilizing a 4-bit flash ADO and a second order requantizer with one bit output implemented in a programmable gate array. The overall loop was configured as a First order delta-sigma converter. A FFT with a Eann window was made on a 4096-point sample taken from the converter running in real time. Fig. 8.



■ Figure 7. *Time response of delta-sigma loop with requantizer in return path for oneand four bit ADC in the forwward path*



■ Figure 8. *Prototype loop*

ACKNOWLEDGEMENTS

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