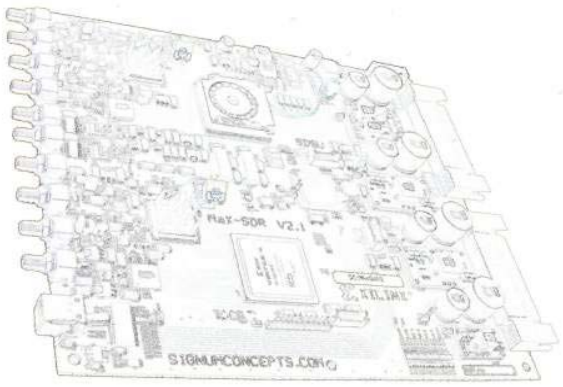

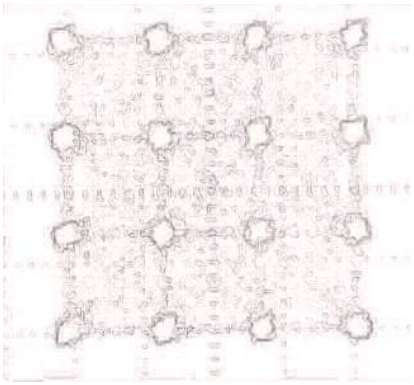

MAX SDR

High Data Rate Modem

Signum Concepts, Inc.

www.signumconcepts.com

MAX SDR High Data Rate Modem

Introduction

The purpose of this document is to describe implementation and operation of **Ultra High Data Rate Modem** developed for **MAX SDR v2.1 FPGA Platform** using high level programming environment System Generator available from Xilinx**.**

Prerequisites

MAX SDR v2.1 FPGA Platform

MATLAB v6.5 or higher

Synplicity Synplify Pro v8.1 or higher

Xilinx ISE v8.1 or higher

Overview

MAX SDR High Data Rate Modem is reference design for direct RF down conversion applications. Reference modem is implemented on *Signum Concepts* MAX SDR v2.1 FPGA Board. Modem is using QPSK or QAM 16 modulation schemes to transfer user data. Incoming user data stream is sampled at receiver side using "state-of-the-art" 3 GSPS 8-bit A/D converter. Sampling is done directly on high IF center frequency 375 MHz. Data bandwidth occupies frequencies from 375-187.5MHz to 375+187.5MHz. Raw data rate varies from **375Mbps** (QPSK) up to **750Mbps** (QAM16). One MAX SDR FPGA Board has sufficient resources for stand-alone test implementation of both

modulator and demodulator sides with separate clock entities. In that way single board modem test setup will be equivalent to test performed on two hardware platforms.

Implemented streaming modem solves following transmission problems:

- sampling (timing) offset
- frequency offset
- phase offset
- automatic gain control (AGC)
- channel distortion

Implementation

MAX SDR High Data Rate Modem is designed using System Generator v8.1 and capabilities of DSP48 dedicated lines and blocks embedded in XIlinx Virtex-4. Due to highly efficient implementation design natively runs on 375 MHz.

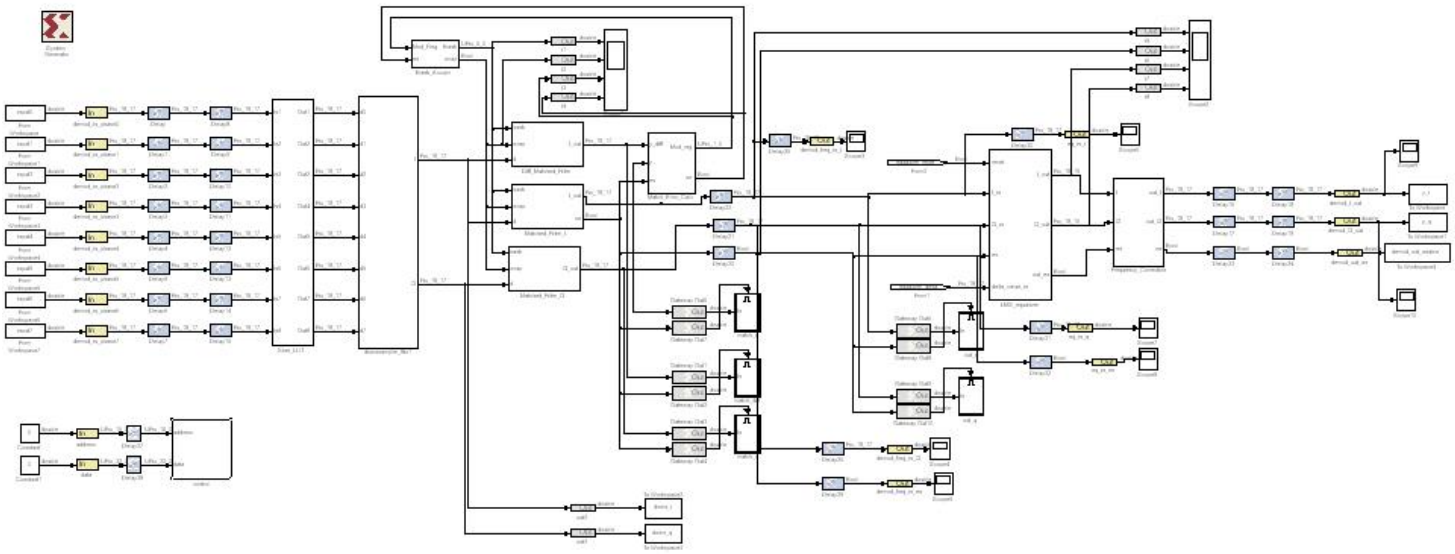

Figure 1 Demodulator Design – Simulink Test Environment

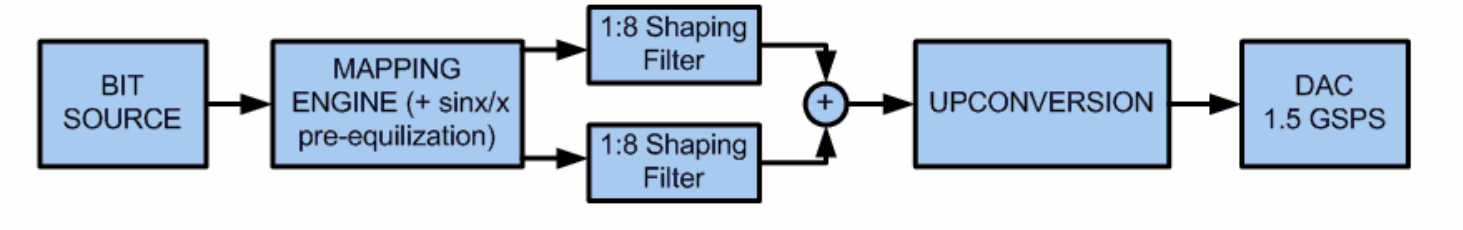

Figure 2 Modulator – basic block diagram

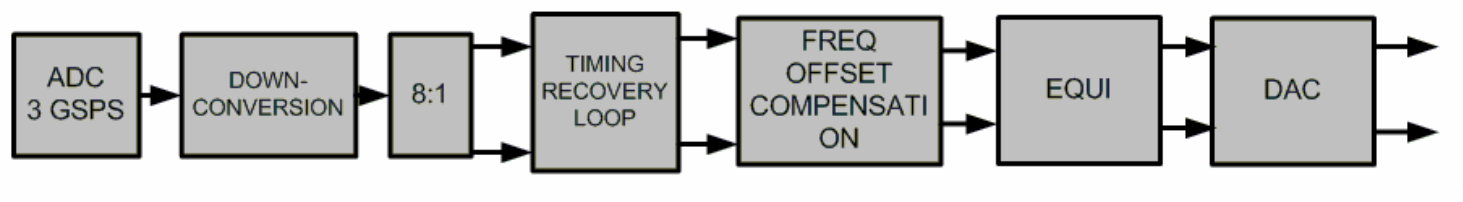

Figure 3 Demodulator – basic block diagram

	Slices	BRAM	DSP48
Virtex-4 SX-55	24576	320	512
DEMODULATOR	4569	33	161
Used Resources	**19%**	**10%**	**31%**

Figure 4 Summary of FPGA resources utilized by demodulator design

Hardware Test Setup

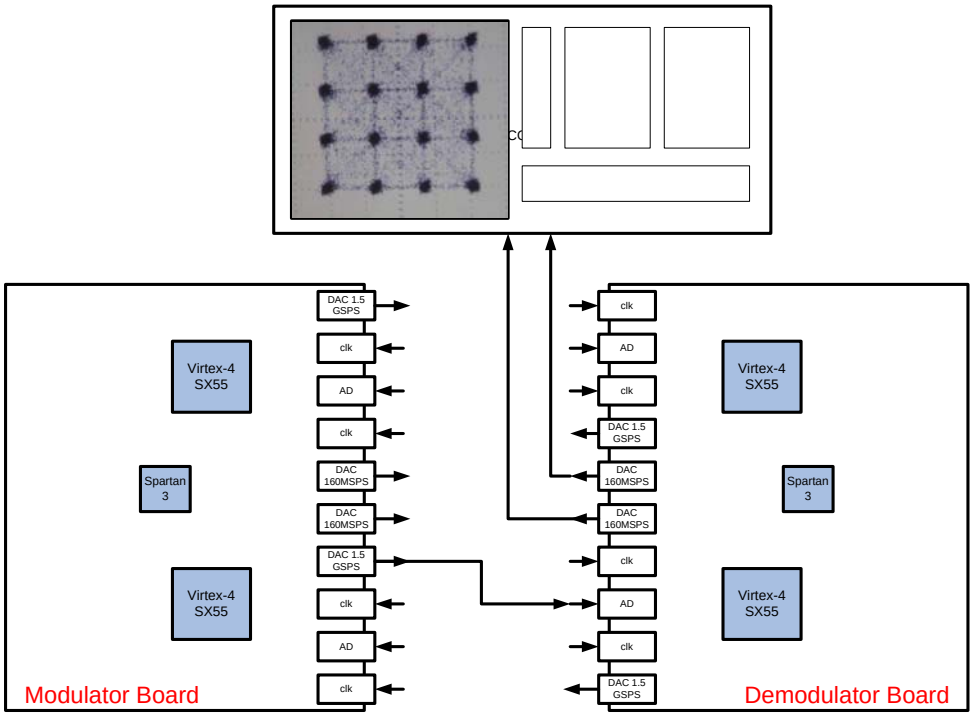

Figure 5 Example of modem test setup

Performance Review

For performance review purposes, demodulated user data are transferred through USB port to MATLAB environment.

Logged constellation diagrams for both QPSK and QAM16 modulation schemes are given on following figures. Results are comparable with constellation diagram gathered on scope.