

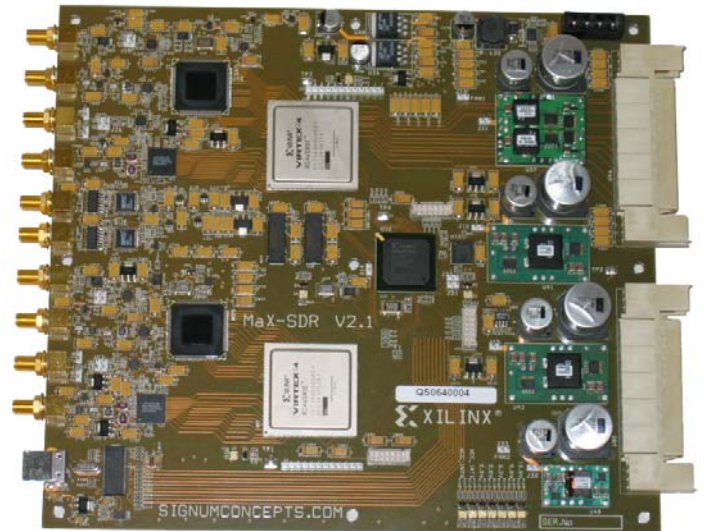
High Speed A/D and D/A Software Defined Radio Development Platform V2.1,
July 15th, 2006

Overview

MAX SDR v2.1 is FPGA-based SDR development platform, based on Xilinx Virtex-4 technology and high speed analog to digital and digital to analog converters.

It lends itself to various applications requiring very high speed data conversion and massive DSP processing engine.

High speed USB 2.0 interface and personality module connection to ML410 Xilinx development platform enable user to minimize the development time and focus attention to the problem at hand, and not on development environment.



Key Features

- *Personality module connection to ML410*
- *USB 2.0 support via Spartan 3 firmware*
- *2 Xilinx Virtex 4 SX55 User FPGAs*
- *2 ADC channels – 8 bits @ 3Gsp/s*
- *2 DAC channels – 12 bits @ 1.5Gsp/s*
- *2 DAC channels – 14 bits @ 160Msp/s*
- *Programmable and flexible clock scheme*

Advantages

- *Ultra high speed analog I/O connected directly to FPGA resources, thus enabling user to process RF data*
- *High speed interface support for development time reduction and advanced debugging*
- *Biggest and fastest processing power from state of the art Xilinx Virtex-4 generation of FPGAs.*

Specifications

Processing engine

- *Two Xilinx Virtex 4 SX55 FPGA -12 with five million equivalent gates ideally suited for intensive DSP*
- *Xilinx Spartan 3 1500 FPGA – 5 with million and a half equivalent gates ideally suitable for interface firmware and control purposes*

Analog I/O

- *two high speed ADCs - 8bit @3Gsp/s; input programmable gain amplifiers; National Semiconductor ADC083000 ADCs*
- *two high speed DACs - 12bit 2.3 Gsp/s; line driver amplifiers on output; Maxim*

Semiconductors MAX19692 DACs (default rate 1.5Gsp/s)

- 2 additional output channels for debugging purposes; line driver operational amplifiers on output; 2 Analog devices AD9772A 14bit 160Msp/s DACs
- 2 External buffered clock sources
- 2 buffered clock outputs
- On board oscillator clock source
- Programmable VCOs for flexible clocking scheme
- single ended analog I/Os with SMA connectors

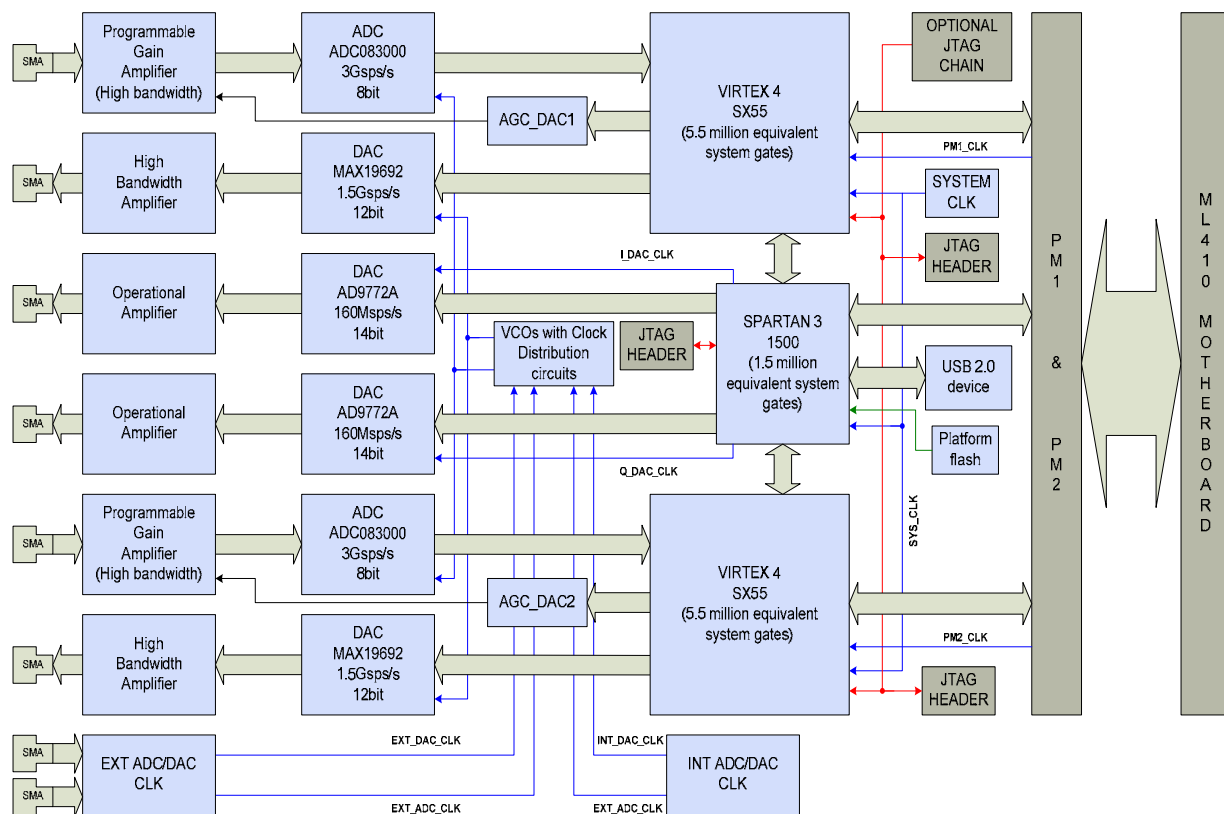
Power

- External standard PC power supply through HDD connector
- ML410 power supply through personality module connector

Configuration

- Via USB 2.0 interface
- Via ML410 board
- On board JTAG connectors

Functional Diagram



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